Design and Implementation of Domino Logic Circuit in CMOS

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Abstract – Domino logic is a CMOS-based evolution of the dynamic logic techniques. It allows a rail-to-rail logic swing. It was developed to speed up circuits. In integrated circuit design, dynamic logic (or sometimes clocked logic) is a design methodology in combinatorial logic circuits, particularly those implemented in MOS technology. This work is oriented towards implementing the domino logic circuits and static CMOS logic circuits and comparing these technologies to show that the domino logic technology is much better than static CMOS technology. The proposed methodology is simple in designing; easy to understand and it is very low power technology. In this work, we have designed the various Domino logic gates such as AND, OR, NAND, NOR and here we have analyzed the performance of these gates in the terms of number of transistors, area, and Power.

Index Terms – VLSI, Static CMOS, Dynamic CMOS, Domino logic, MOSFET, Simulation.

1. INTRODUCTION

In integrated circuit design, dynamic logic is a design methodology in combinatorial logic circuits, particularly those implemented in MOS technology. Dynamic logic circuits are usually faster than static counterparts, and require less surface area, but are more difficult to design, and have higher power dissipation. Domino logic circuit techniques are extensively applied in high-performance microprocessors due to the superior speed and area characteristics of dynamic CMOS circuits as compared to static CMOS circuits. High-speed operation of domino logic circuits is primarily due to the lower noise margins of domino circuits as compared to static gates. Domino logic offers speed and area advantages over conventional static CMOS and is especially useful for implementing complex logic gates with large fan-outs.

A. Static CMOS

A static CMOS logic network is composed of static CMOS gates which are a combination of two networks a pull-up network, consisting of PMOS transistors, connected to power, and a pull-down network, consisting of NMOS transistors, connected to ground. Static CMOS logic is common in ASIC design, where the extra design cost of higher performance logic is often not justified by the relatively low volumes, and where ultimate performance is often not required. The simplicity of static CMOS generally leads to relatively low power dissipation, especially for low fan-in gates

B. Domino Logic

Domino logic is one of the most effective circuit configurations for implementing high speed logic designs. Domino circuits offer the advantages of faster transitions and glitch-free operation. Domino logic is a CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. It runs 1.5-2 times faster than static CMOS logic because dynamic gates present much lower input capacitance for the same output current and a lower switching threshold. In Domino logic a single clock is used to precharge and evaluate a cascaded set of dynamic logic blocks.

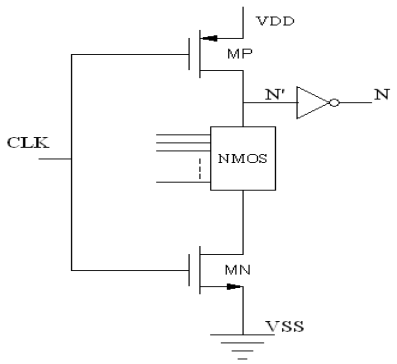

Figure 1: A Domino Logic Circuit

2. RELATED WORK

Dynamic logic requires two phases, the first phase is set up phase or precharge phase, in this phase the output is unconditionally go to high (no matter the values of the inputs A and B). The capacitor which represents the load capacitance

of this gate becomes charged. During the evaluation phase, CLK is high.

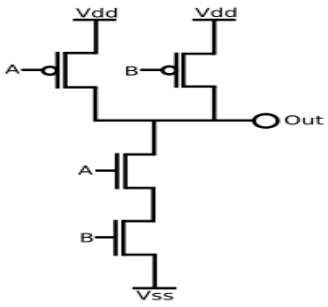

Figure 2: Example of static logic NAND gate

Domino logic is a CMOS based evaluation of the dynamic logic techniques which are based on the either PMOS or NMOS transistors. The dynamic gate outputs connect to one inverter, in domino logic. In domino logic, cascade structure consisting of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to "1" (until the next CLK cycle), just as dominos, once fallen, cannot stand up. The structure is hence called Domino CMOS logic.

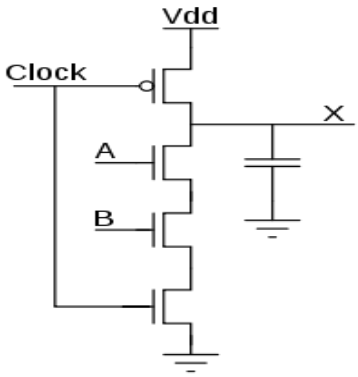

Figure 3: Example of Dynamic logic NAND gate

3. PROPOSED MODELLING

In Dynamic Logic, a problem arises when cascading one gate to the next. The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, so there is no recovery from this error. While this might seem to defeat the point of dynamic logic, since the inverter has a PFET (one of the main goals of Dynamic Logic is to avoid PFETs where possible, due to speed), there are two reasons it works well. First, there is no fan-out to multiple PFETs.In a domino logic cascade structure consisting of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to "1" (until the next clock cycle) just as dominos, once fallen, cannot stand up. The structure is hence called Domino CMOS Logic.

4. RESULTS AND DISCUSSIONS

Here in the implementation of static CMOS, we designed the basic gates such as INVERTER, AND, NAND, OR and NOR. The implementation is done with the help of Berkeley Short Channel Igfet Model (BSIM4) and transient. The design and simulation of the gates are shown below.

1. INVERTER .

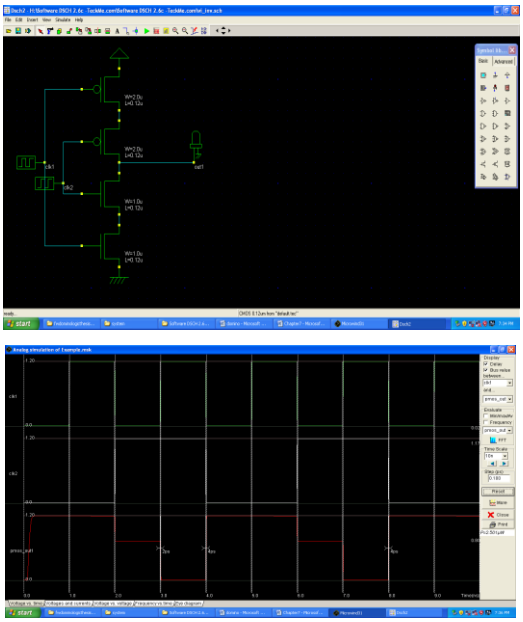

Figure 4 : Simulation result for inverter

2.AND Gate

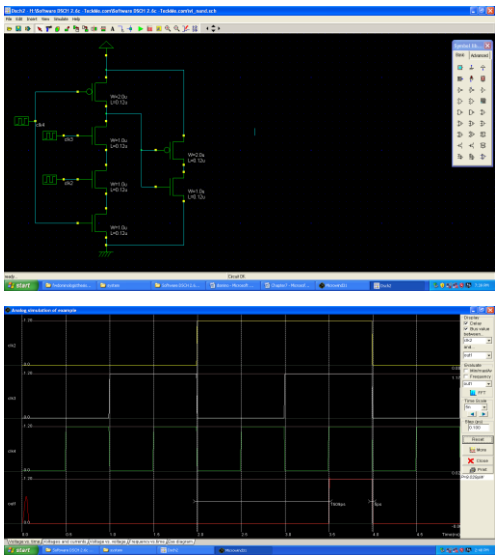

Figure 5 : simulation result for AND gate

3.NAND Gate

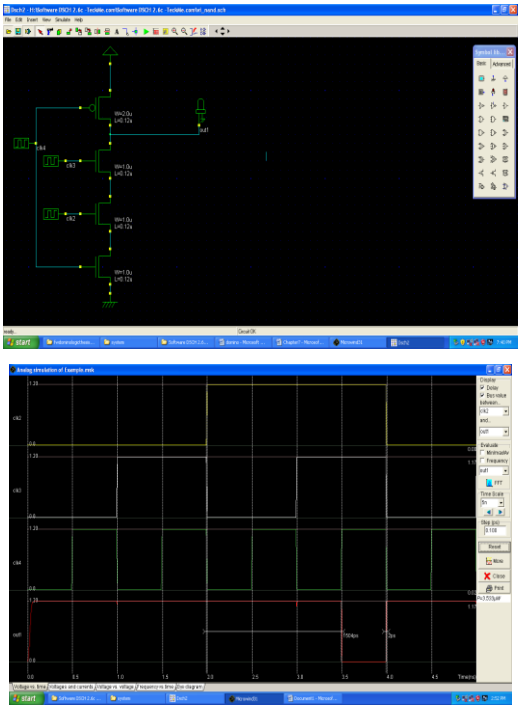

Figure 6 : Simulation result for NAND gate

4. OR Gate

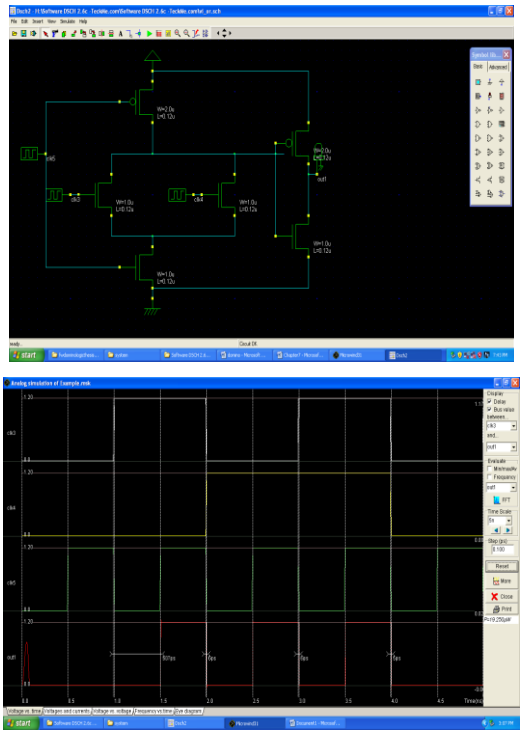

Figure 7: Simulation result for OR gate

5. NOR Gate

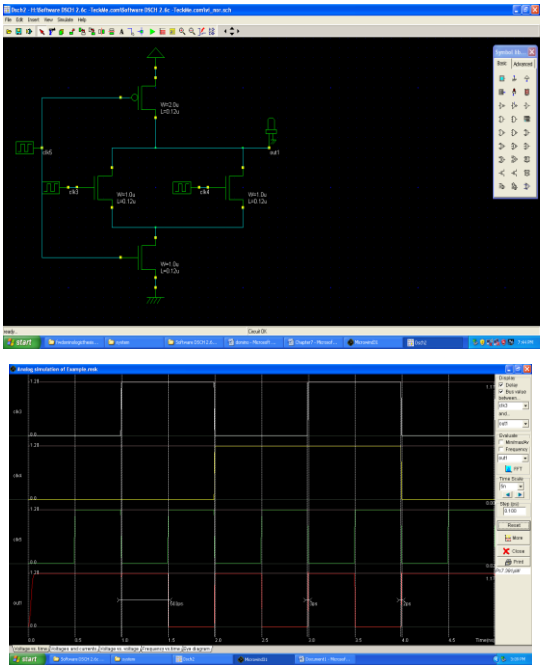

Figure 8: Simulation result for NOR gate

5. CONCLUSION

Simulation of gates was done on Microwind software and DSCH. The simulation result shows that for an OR gate, the delay has reduced from 15ps to 5 ps when implemented in Domino logic. Thus Domino logic can be used in implementing high speed logic designs. Domino circuits offer the advantages of faster transitions and glitch-free operation. The detailed simulation result is shown in the following table.

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Sr. No.	Circuits	Static CMOS Logic			Domino Logic		
		Transistor Count	Delay	Power Dissipation	Transistor Count	Delay	Power Dissipation
1	**Inverter**	2	2ps	3.132uW	4	4p	2.501u
2	**NAND**	4	2ps	3.132uW	4	2ps	3.53u
3	**AND**	6	6ps	9.8uW	6	5ps	9.029u
4	**OR**	6	15ps	10.259uW	6	5ps	19.250u
5	**NOR**	4	7ps	3.924uW	4	2ps	7.391u